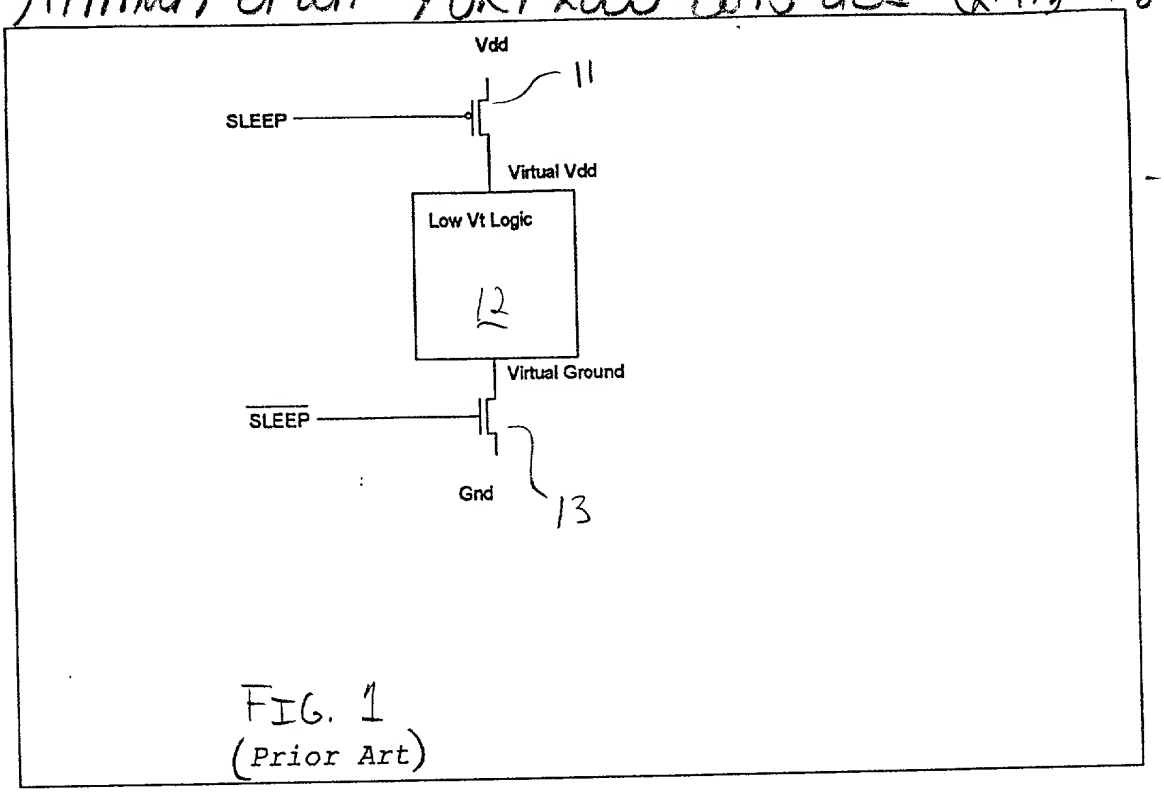


FIG. 1
(Prior Art)

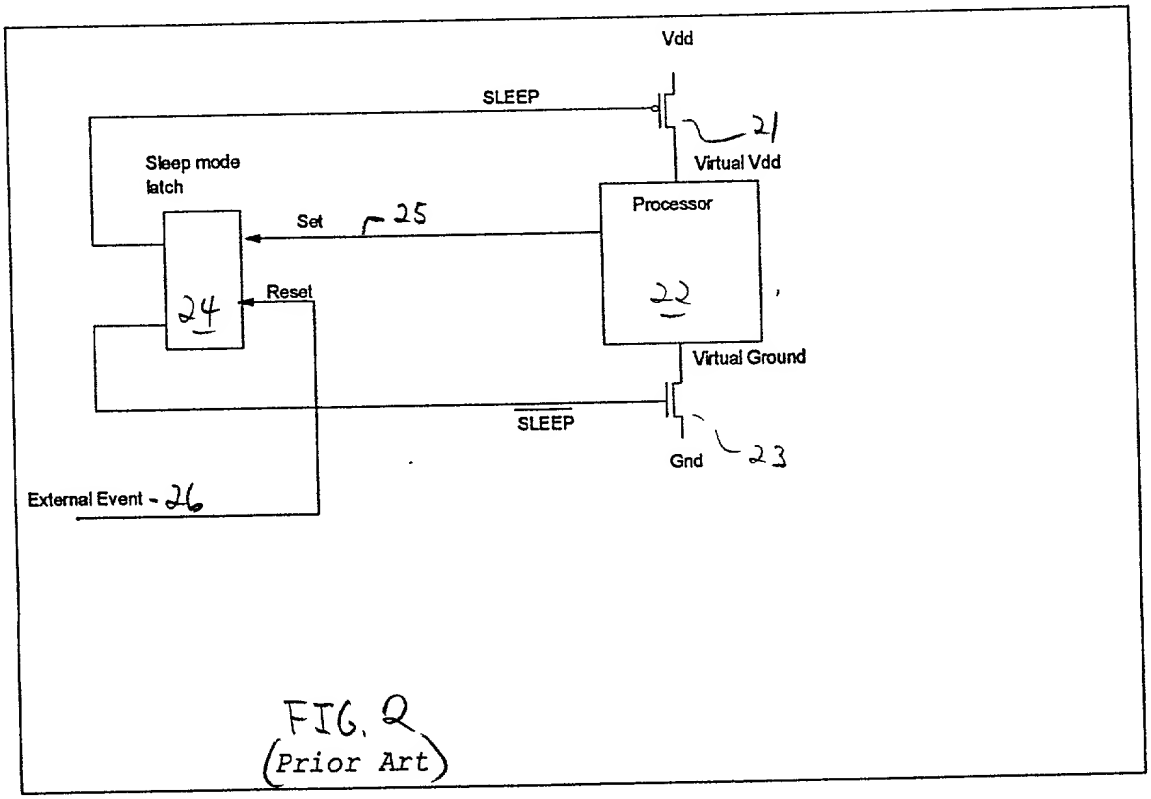


FIG. 2
(Prior Art)

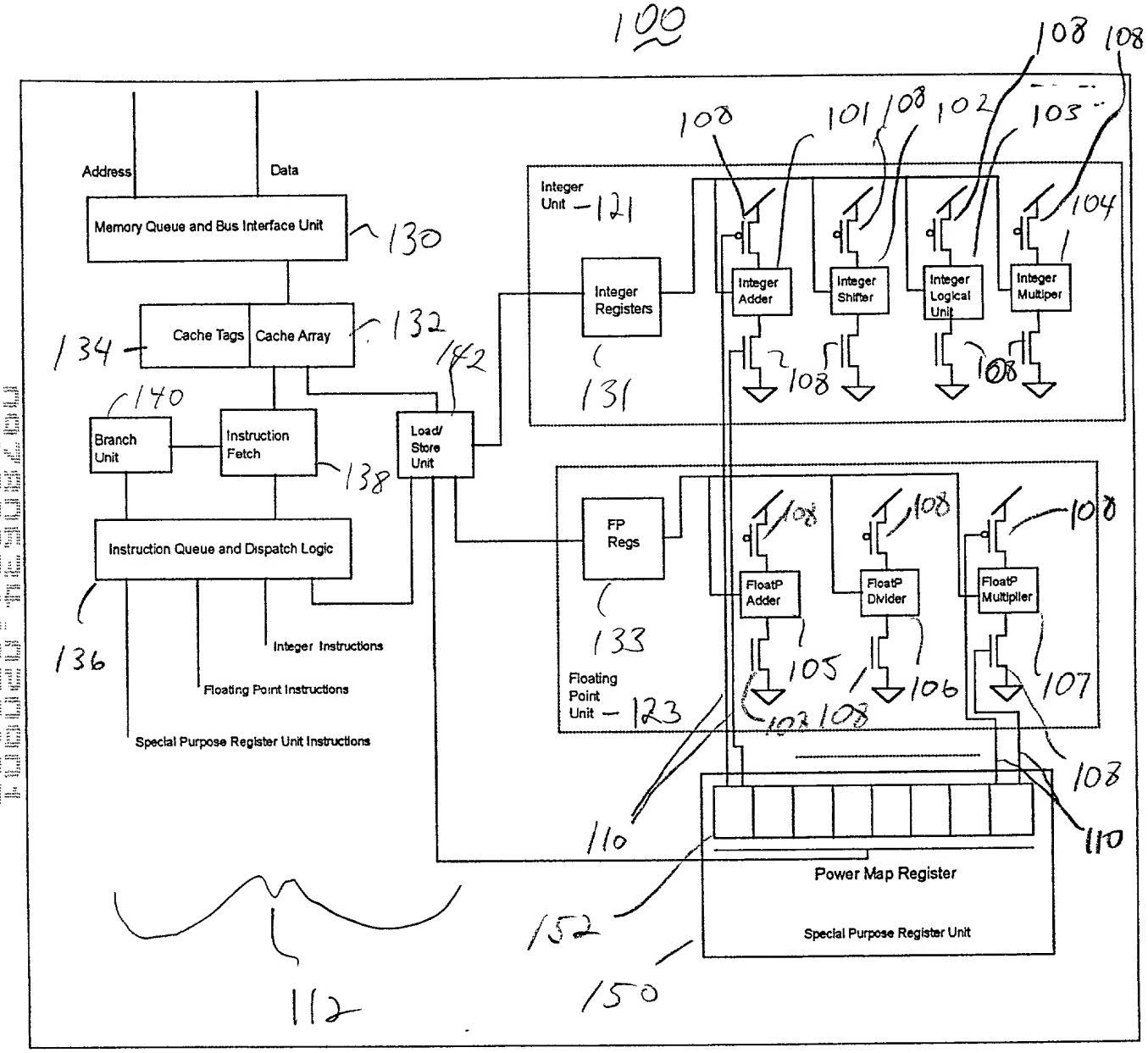
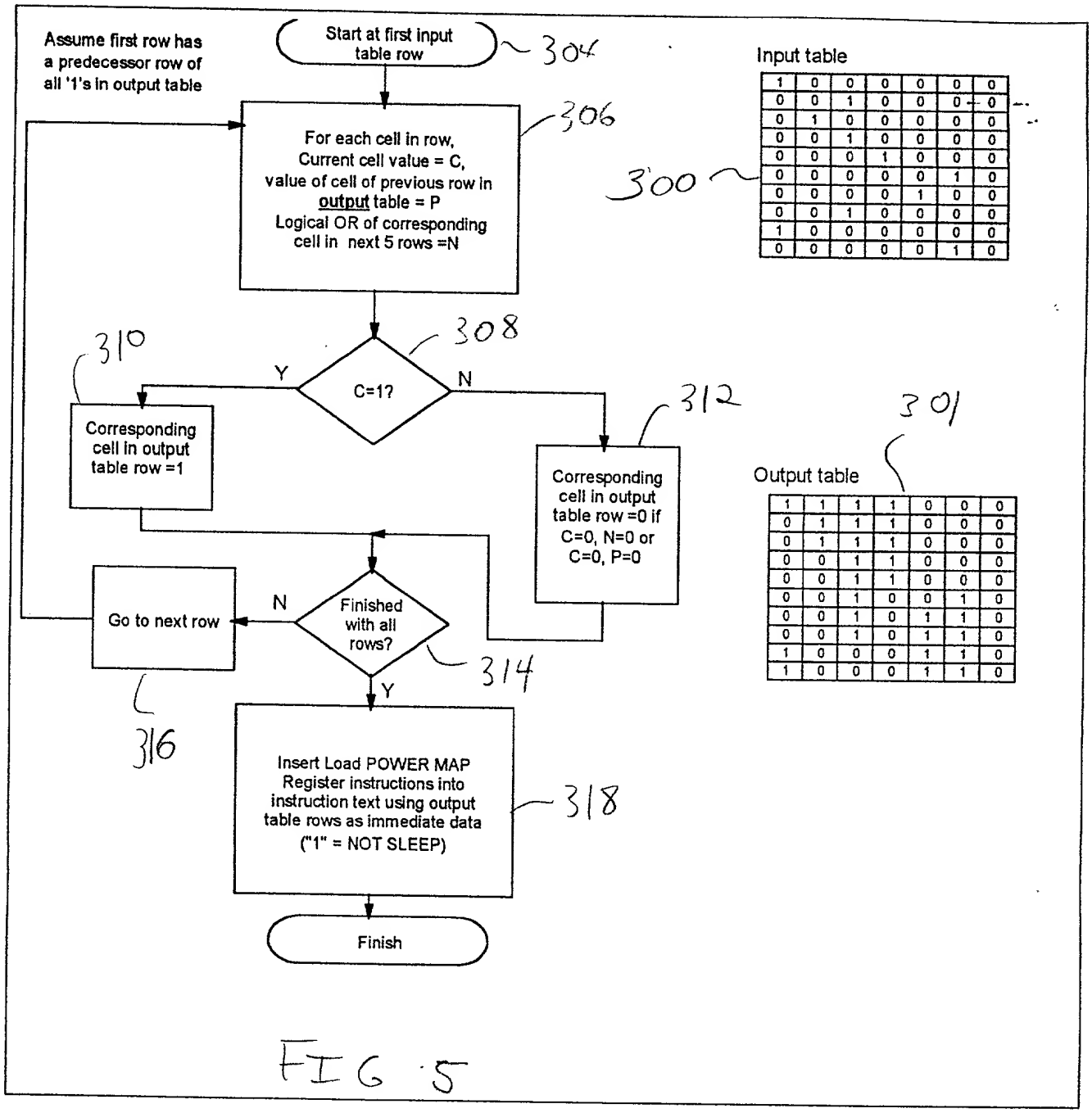

100
Address
Data
Memory Queue and Bus Interface Unit
130
Cache Tags
Cache Array
132
134
142
140
Branch Unit
Instruction Fetch
138
Load/ Store Unit
Instruction Queue and Dispatch Logic
136
Integer Instructions
Floating Point Instructions
Special Purpose Register Unit Instructions
Integer Unit
121
Integer Registers
131
Integer Adder
Integer Shifter
Integer Logical Unit
Integer Multiper
FP Regs
133
FloatP Adder
FloatP Divider
FloatP Multiplier
Floating Point Unit
123
Power Map Register
Special Purpose Register Unit
110
152
150
112
101
102
103
104
105
106
107
108

FIG. 3



1	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	0	1	0	0	0	0
0	0	0	1	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	1	0	0	0	0
1	0	0	0	0	0	0
0	0	0	0	0	1	0

1	1	1	1	0	0	0
0	1	1	1	0	0	0
0	1	1	1	0	0	0
0	0	1	1	0	0	0
0	0	1	1	0	0	0
0	0	1	0	0	1	0
0	0	1	0	1	1	0
0	0	1	0	1	1	0
1	0	0	0	1	1	0
1	0	0	0	1	1	0

FIG 5

8,000,000 Patented

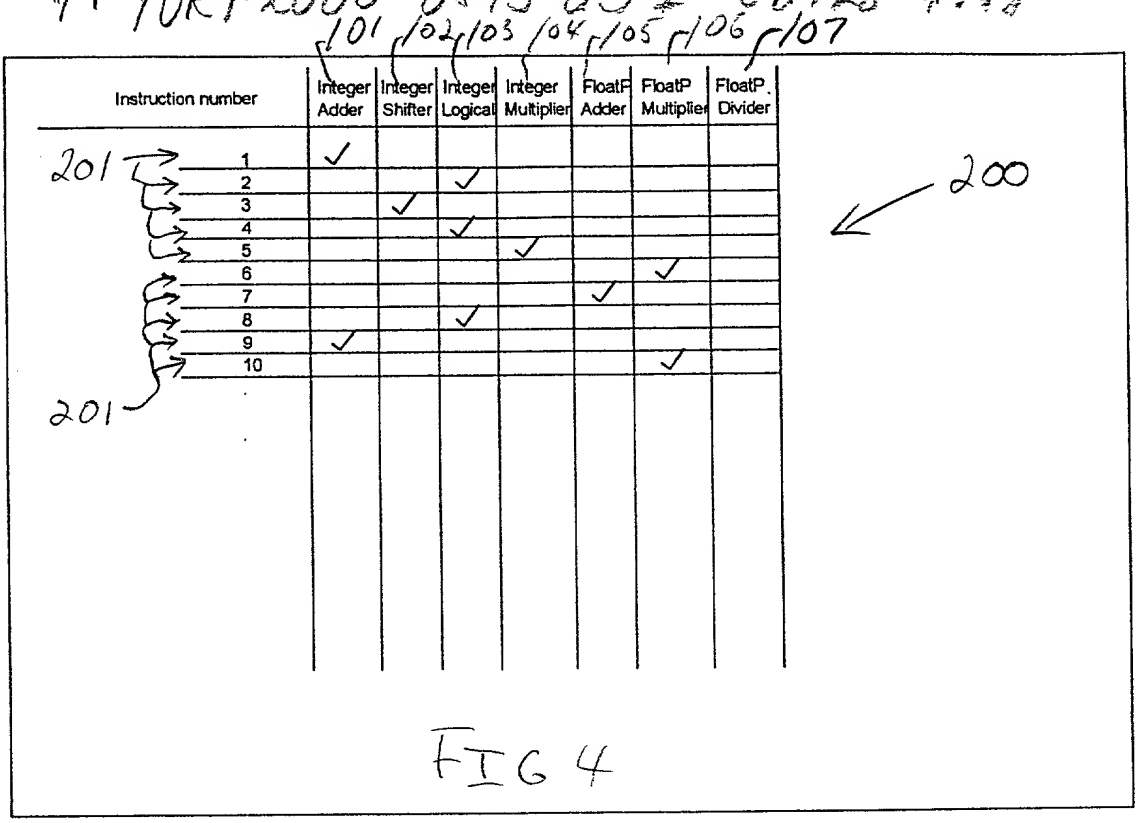


FIG 4

Instruction Sequence

LoadPowerMap 1111000
1
LPM 0111000
2
3
LPM 0011000
4
5
LPM 0010110
6
7
8
LPM 1000110
9
10
.
.
.
.

FIG. 6

EAST Search History